P18396

APPLICATION FOR UNITED STATES LETTERS PATENT

FOR

METHOD AND APPARATUS TO WRITE DATA

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"Express Mail" Label Number: **EL 962029088 US**

METHOD AND APPARATUS TO WRITE DATA

BACKGROUND

One type of memory for storing data and/or code is a flash electrically erasable programmable read-only memory ("flash EEPROM" or "flash memory"). Once programmed, the flash memory may retain its data until the memory is erased. Electrical erasure of the flash memory may include erasing the contents of the memory of the device in one relatively rapid operation. The flash memory may then be programmed with new code or data.

A flash memory may be controlled using commands and control signals such as, for example, a chip select (CS) signal and a write enable signal (WE). The commands may include a read, program or write, and erase commands. The chip enable signal may also be referred to as a chip enable (CE) signal.

Glitch or noise signals may occur on the bus that may cause the WE and CS signals to become asserted inadvertently. This may cause the flash memory to initiate an undesirable or unwanted write operation by latching in unwanted or invalid write commands in the flash memory.

Thus, there is a continuing need for alternate ways to write data to a memory.

BRIEF DESCRIPTION OF THE DRAWINGS

The subject matter regarded as the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The present invention, however, both as to organization and method of operation, together with objects,

features, and advantages thereof, may best be understood by reference to the following detailed description when read with the accompanying drawings in which:

FIG. 1 is a block diagram illustrating a computing system in accordance with an embodiment of the present invention;

FIG. 2 is a timing diagram illustrating a write operation in accordance with an embodiment of the present invention;

FIG. 3 is a block diagram illustrating a computing system in accordance with an embodiment of the present invention;

FIG. 4 is a block diagram illustrating an implementation of the computing system of FIG. 3 in accordance with an embodiment of the present invention;

FIG. 5 is a timing diagram illustrating a write operation;

FIG. 6 is a timing diagram illustrating a write operation in accordance with an embodiment of the present invention; and

FIG. 7 is a block diagram illustrating a wireless device in accordance with an embodiment of the present invention.

It will be appreciated that for simplicity and clarity of illustration, elements illustrated in the figures have not necessarily been drawn to scale. For example, the dimensions of some of the elements are exaggerated relative to other elements for clarity. Further, where considered appropriate, reference numerals have been repeated among the figures to indicate corresponding or analogous elements.

DETAILED DESCRIPTION

In the following detailed description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be understood by those skilled in the art that the present invention may be practiced without these specific details. In other instances, well-known methods, procedures, components and circuits have not been described in detail so as not to obscure the present invention.

In the following description and claims, the terms "include" and "comprise," along with their derivatives, may be used, and are intended to be treated as synonyms for each other. In addition, in the following description and claims, the terms "coupled" and "connected," along with their derivatives, may be used. It should be understood that these terms are not intended as synonyms for each other. Rather, in particular embodiments, "connected" may be used to indicate that two or more elements are in direct physical or electrical contact with each other. "Coupled" may mean that two or more elements are in direct physical or electrical contact. However, "coupled" may also mean that two or more elements are not in direct contact with each other, but yet still co-operate or interact with each other.

FIG. 1 is a block diagram illustrating a computing system 100 in which embodiments of the present invention may be used. System 100 may include a processor 110 and a flash memory 120 coupled to processor 110.

Although not shown, system 100 may include other components such as, for example, more processors, input/output (I/O) devices, storage devices, or other memories such as, for example, a cache memory. In addition, system 100 may include other peripheral interfaces or controllers such as, for example, a liquid crystal display (LCD) controller or a camera interface. However, for simplicity these additional components have not been shown.

Flash memory 120 may be a NAND or NOR type of flash memory, and may be a single bit per cell or multiple bits per cell memory. Flash memory 120 may store software instructions and/or data. The terms "data" or "information" may be used to refer to either data, instructions, or code. Processor 110 may include logic to execute software instructions and may also be referred to as a core, a controller or a processing unit. Processor 110 may also include a memory controller or a circuit or circuitry such as, for example, digital logic to control memory accesses to flash memory 120.

In one embodiment, processor 110 may include a write state machine (WSM) (not shown) to manage erasing of, and writing to, flash memory 120. The WSM may generate the commands and control signals to write to flash memory 120. For example, control signals nCS, nWE, and nOE may be generated by the WSM of processor 110. The "n" prefix may indicate that these signals are active low signals. In other words, these signals are asserted when they are at a relatively "low" voltage level of for example, about zero volts, and are deasserted when they are at a relatively "high"

voltage level of, for example, about two volts.

As discussed above, CS and WE are chip select and write enable signals, respectively. OE is an output enable signal that may be the output control signal for flash memory 120. In one example, when OE is deasserted, the device outputs of flash memory 120 may be disabled and placed in a high impedance (high-z) state. During a write operation, processor 110 may provide or send several bits or bytes of data and an address to flash memory 120, wherein the address is the location in flash memory 120 where the data is to be written. The nCS, nWE, and nOE signals may be respectively coupled to a chip select pin, a write enable pin, and an output enable pin of flash memory 120.

Turning to FIG. 2, shown is a timing diagram illustrating a write operation to flash memory 120 in accordance with an embodiment of the present invention. In this embodiment, all write operations may be asynchronous, so that the clock (not shown) to the memory may be ignored. To perform a write operation, both nCS and nWE may be asserted while nOE may be deasserted.

As is illustrated in FIG. 2, in one embodiment writing data to flash memory 120 may begin with transmitting or sending the write address to flash memory 120. Next, the nWE signal may be asserted and the nCS signal may be asserted after the asserting of the nWE signal. Then, the nCS signal may be deasserted to latch the data and the address in flash memory 120, wherein the deasserting of the nCS signal occurs after the asserting of the nWE signal. Next, the nWE signal may be deasserted after the deasserting of the nCS signal.

In this embodiment, the address and data are latched in flash memory 120 on

the rising edge of the nCS signal, i.e., the address and data are latched in flash memory 120 on the deasserting of the nCS signal. The data and address may be sent to flash memory 120 anytime prior to the deasserting of the nCS signal. During the entire write operation, nOE may be deasserted.

Although nWE is illustrated as being asserted prior to the asserting of nCS, this is not a limitation of the present invention. In an alternate embodiment, nCS may be asserted prior to nWE. In addition, although the CS and WE signals are illustrated as active low, in an alternate embodiment, the CS and WE signals may be active high signals and the address and data may be latched on a falling edge of CS rather than a rising edge as is illustrated in FIG. 2. It should be pointed out that the times shown at the top of FIG. 2 are only one example, and the present invention is not limited in this respect.

If commands are used, a write operation may include two back-to-back writes, wherein the data and address sent to flash memory 120 during the first write may include the command and the data and address sent to flash memory 120 during the second write may include the data to be written.

Turning to FIG. 3, shown is a block diagram illustrating a computing system 200 in accordance with an embodiment of the present invention. System 200 may include processor 110, flash memory 120, and a flash memory 130. In this embodiment, the nWE and nOE signals are shared between multiple flash memories, i.e., are shared between flash memory 120 and flash memory 130. In other words, the nWE signal is coupled to at least two memories, e.g., the nWE signal may be coupled to both the write enable pin of flash memory 120 and to the write enable pin of flash memory 130.

Similarly, the nOE signal is coupled to at least two memories, e.g., the nOE signal may be coupled to both the output enable pin of flash memory 120 and to the output enable pin of flash memory 130. Sharing control signals may reduce the number of pins on processor 110.

Dedicated CS signals may be used in computing system 200, e.g., a dedicated nCS_0 signal may be coupled to the chip select pin of flash memory 120 and a dedicated nCS_1 signal may be coupled to the chip select pin of flash memory 130.

As an example, one problem that may occur by sharing signals is if flash memory 120 is physically close to processor 110 (e.g., if flash memory 120 is a discrete die stacked on the processor 110 die), and flash memory 130 is farther away from processor 110 (e.g., the flash memory 130 die is not stacked on processor 110 die), the shared control signals may experience some signal integrity issues, e.g. reflection on the signals such that what is seen is not predictable and erroneous edges may occur on the signals that may cause inadvertent writes. To overcome this problem, writing to flash memories 120 and 130 may be accomplished using the method illustrated in FIG. 2. Specifically, in one embodiment, during a write operation, the data and address sent to either flash memory 120 or 130 is latched in the memory on the deassertion of the dedicated chip select signal rather than on the deassertion of the shared write enable signal. In other words, the write to a flash memory (e.g., 120 or 130) of system 200 may occur on the rising edge of the dedicated chip select signal (e.g., nCS_0 or nCS_1) rather than on the rising edge of the shared write enable signal (e.g., nWE). This may allow the dedicated chip select signal to be the controlling signal during a write operation and may allow for any reflection on the shared write enable signal to not

affect the system.

One solution to the problem of reflection of signals may be to include a terminator circuit or matching circuit near an end of the wire. However, including a matching or terminator circuit may increase power consumption.

Although system 200 is illustrated as having only two flash memories, this is not a limitation of the present invention. In other embodiments, system 200 may have more than two memories. Further, although memories 120 and 130 are illustrated above as nonvolatile flash memories, this is not a limitation of the present invention. In other embodiments, memories 120 and 130 may be volatiles memories such as, for example, a static random access memory (SRAM) or a dynamic random access memory (DRAM) that may share write enable signals. In addition, in another embodiment, flash memories 120 and 130 may be another type of nonvolatile memory such as, for example, a read only memory (ROM).

Turning to FIG. 4, shown is a block diagram illustrating an implementation of computing system 200 in accordance with an embodiment of the present invention. For simplicity, the data, address, and output enable signals illustrated in FIG. 3 are not shown in FIG. 4.

FIG. 4 illustrates one implementation of processor 110 to generate signals nCS_0, nCS_1, and nWE. In this implementation, processor 110 may include multiplexers 140, 150, and 160 to generate signals nCS_0, nWE, and nCS_1, respectively. This implementation may be used if the internal write state machine of processor 110 is designed to cause the write to occur on the deassertion of nWE rather than on the deassertion of nCS, i.e., to latch the data and address on the rising edge of

nWE. For example, briefly turning to FIG. 5, shown is an example of the internal control signals generated by the internal write state machine, wherein the internal write state machine is designed to cause the write to occur on the deassertion of nWE rather than on the deassertion of nCS.

Multiplexers 140, 150, and 160 may be added to processor 110 to alter or swap the functionality of the CS and WE signals to cause the write to occur on the deassertion of one of the dedicated chip select signals (nCS_0 or nCS_1) rather than on the deassertion of the shared write enable signal. This may be desirable when one of the flash memories is a stacked memory and the other is not. The "i" prefix may indicate that the signal is a signal generated internal to processor 110, e.g., generated by the write state machine of processor 110.

A bit, or several bits, may be used to select the algorithm for transferring or writing data to the flash memories of system 200. For example, a bit may be programmed to enable either latching of the data in a flash memory on the deasserting of the chip select signal or enable latching of the data in a flash memory on the deasserting of the write enable signal.

In one embodiment, the bit used may be a bit to indicate whether or not at least one of the flash memories of system 200 is a stacked flash. If set, the bit may indicate that one of the flash memories is stacked, and then this indication may be used as the selection input to multiplexers 140, 150, and 160 to select which of the plurality of internally generated control signals is transferred externally to flash memories 120 and 130. If set, the external control signals may be generated as shown in FIG. 6 based on the internal signals shown in FIG. 5.

Turning to FIG. 7, shown is a block diagram illustrating a wireless device 400 in accordance with an embodiment of the present invention. In one embodiment, wireless device 400 may use the methods discussed above and may include a computing system 410. Computing system 410 may be computing systems 100 or 200 that is discussed above with reference to FIGS. 1-6.

As is shown in FIG. 7, wireless device 400 may include an antenna 420 coupled to a processor of system 410 via a wireless interface 430. In various embodiments, antenna 420 may be a dipole antenna, helical antenna or another antenna adapted to wirelessly communicate information. Wireless interface 430 may be adapted to process radio frequency (RF) and baseband signals using wireless protocols and may include a wireless transceiver.

Wireless device 400 may be a personal digital assistant (PDA), a laptop or portable computer with wireless capability, a web tablet, a wireless telephone (e.g., cordless or cellular phone), a pager, an instant messaging device, a digital music player, a digital camera, or other devices that may be adapted to transmit and/or receive information wirelessly. Wireless device 400 may be used in any of the following systems: a wireless personal area network (WPAN) system, a wireless local area network (WLAN) system, a wireless metropolitan area network (WMAN) system, or a wireless wide area network (WWAN) system such as, for example, a cellular system.

An example of a WLAN system includes a system substantially based on an Industrial Electrical and Electronics Engineers (IEEE) 802.11 standard. An example of a WMAN system includes a system substantially based on an Industrial Electrical and

Electronics Engineers (IEEE) 802.16 standard. An example of a WPAN system includes a system substantially based on the Bluetooth™ standard (Bluetooth is a registered trademark of the Bluetooth Special Interest Group). Another example of a WPAN system includes a system substantially based on an Industrial Electrical and Electronics Engineers (IEEE) 802.15 standard such as, for example, the IEEE 802.15.3a specification using ultrawideband (UWB) technology.

Examples of cellular systems include: Code Division Multiple Access (CDMA) cellular radiotelephone communication systems, Global System for Mobile Communications (GSM) cellular radiotelephone systems, Enhanced data for GSM Evolution (EDGE) systems, North American Digital Cellular (NADC) cellular radiotelephone systems, Time Division Multiple Access (TDMA) systems, Extended-TDMA (E-TDMA) cellular radiotelephone systems, GPRS, third generation (3G) systems like Wide-band CDMA (WCDMA), CDMA-2000, Universal Mobile Telecommunications System (UMTS), or the like.

Although computing systems 100 and 200 are illustrated as being used in a wireless device in one embodiment, this is not a limitation of the present invention. In alternate embodiments systems 100 and 200 may be used in non-wireless devices such as, for example, a server, a desktop, or an embedded device not adapted to wirelessly communicate information.

While certain features of the invention have been illustrated and described herein, many modifications, substitutions, changes, and equivalents will now occur to those skilled in the art. It is, therefore, to be understood that the appended claims are intended to cover all such modifications and changes as fall within the true spirit of the invention.